REMARKS

The present application was filed on February 20, 2002 with claims 1-26, claiming the priority of U.S. provisional patent application Serial No. 60/270,263 filed February 21, 2001. Claims 1-26 are currently pending in the application. Claims 1, 5, 9 and 18 are the independent claims.

In the third and final Office Action, claims 1 and 5 are rejected under 35 U.S.C. §102(a) as being anticipated by Heijningen et al., *Analysis and Experimental Verification of Digital Substrate Noise Generation for Epi-Type Substrates*, IEEE Journal of Solid-State Circuits, Vol. 35, No. 7 (July 2000) (hereinafter "Heijningen"). In addition, claims 9-11, 13, 18-20, 22 and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 6,135,649 to Feldmann et al. (hereinafter "Feldmann") in view of U.S. Pat. No. 6,075,770 to Chang et al. (hereinafter "Chang").

The Examiner has indicated that claims 2-4, 6-8, 12, 14-17, 21 and 24-26 would be allowable if rewritten in independent form.

Before addressing the specific rejections, Applicants wish to point out that the Examiner responds to the Applicants' response to the second Office Action by stating:

> The Examiner agrees that the reference includes both measurements and simulating of devices, but because the general nature of the all (*sic*) the claims as written, proper prosecution and preferred direction of this application still rests in the direction of allowable subject matter.

Applicants, unfortunately, are uncertain what the Examiner means by this statement. For example, Applicants do not understand the reference to the "general nature" of the claims, and the reference to the "preferred direction" of the application. Applicants, therefore, are unable to fully respond to this statement in these remarks.

In this response, Applicants traverse the §102(a) and §103(a) rejections. Applicants respectfully request reconsideration of the present application in view of the following remarks.

With respect to anticipation under §102(a), Applicants generally note that the Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either

expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claims 1 and 5 each comprise elements wherein the performance of an integrated circuit having an analog unit, a digital unit, and a substrate on which the units are located is simulated using "a lumped circuit in which the source [representing noise characteristics of the digital unit] couples to a lumped element representing the substrate and the substrate couples to a lumped element representing the analog unit." These claims, therefore, describe a model for carrying out simulations comprising "lumped" elements. For example, as part of the model, a lumped element representing an analog unit may be coupled to a lumped element representing the substrate in order to determine the effect of noise emitted by one or more digital circuits on one or more analog circuits in a mixed analog and digital integrated circuit. See the Specification, p. 2, lines 27-31; p. 3, lines 23-25; p. 6, lines 4-9; and FIG. 2, element 204.

The Examiner, in formulating the §102(a) rejection, argues that each and every element of claims 1 and 5 is anticipated by Heijningen. More specifically, the Examiner argues that the model comprising a substrate coupled to a lumped element representing an analog unit is described in Heijningen Sect. IV(a), 2nd Paragraph (Office Action, p. 2). Applicants respectfully disagree. Heijningen uses a model for simulating substrate noise comprising three mechanisms: coupling from a digital power supply, coupling from switching source-drain nodes, and impact ionization in a MOSFET channel (Heijningen, Sec. III, 2nd Paragraph). Unlike claims 1 and 5, Heijningen does not describe a model comprising a lumped element representing an analog unit coupled to a substrate.

Moreover, Heijningen, Sect. IV(a), 2nd Paragraph comes from a subsection entitled: "Substrate Noise Measurement Techniques." It states:

> A continuous-time direct measurement technique is the use of an analog differential amplifier, with one input connected to the substrate and the other to quiet reference signal

[14], [15]. The sensor presented in [14], however, has only a limited bandwidth, and measurement of actual coupling from switching digital nodes is not possible due to this bandwidth limitation. A method for accurate measurement of the substrate noise up to 1 GHz, as presented in [15], is analyzed in more detail below.

This paragraph describes tangible analog circuitry to be used for measuring the electromagnetic noise produced by existing digital circuits. Heijningen uses these types of measurement devices to physically verify his simulations of substrate noise (Heijningen, Sec. I, 3rd Paragraph, and Sec. IV, 1st Paragraph). One skilled in the art will immediately recognize that this portion of the reference describes a technique for physically measuring existing devices as opposed to a technique for simulating devices in the manner claimed.

Furthermore, with respect to the §102(a) rejection of claims 1 and 5, the Examiner adds in the most recent Office Action (p. 4) that a "[s]imulation of substrate noise is accomplished using a lumped element (Fig. 6) and analog signals (Heij. Pg. 1005 1st para)." Applicants respectfully assert that the Examiner is again applying a technique for physically measuring existing devices to a technique for simulating devices in the manner claimed. The "analog signals" that the Examiner references at Heijningen, p. 1005, 1st paragraph, are actual analog signals used to physically measure an existing device. These analog signals are, therefore, not utilized in a simulation.

Based on these differences, Applicants respectfully submit that all the elements of claims 1 and 5 are not described by Heijningen, and that the claims should, therefore, be allowed.

With respect to the §103(a) rejections of 9-11, 13, 18-20, 22 and 23, Applicants begin by noting that 37 C.F.R. §1.104(c)(2) requires that, in rejecting claims for want of novelty or for obviousness, "[w]hen a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable." Applicants further note that MPEP §706.02(i) states that, when making a rejection, "the particular part of a reference relied upon to support the rejection should be identified." Applicants observe that, although these requirements were pointed out by the Applicants in their preceding response, the Examiner made no changes or additions to the language of the §103(a) rejection in the most recent Office Action. Applicants, therefore, respectfully submit that the §103(a) rejection remains procedurally deficient under the requirements set forth in the Federal Rules and the MPEP.

With regard to §103(a) rejection of claims 9-11, 13, 18-20, 22 and 23. Applicants also note that a proper *prima facie* case of obviousness requires that the cited references, when combined, must "teach or suggest all the claim limitations," and that "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." See MPEP §706.02(j).

In formulating the §103(a) rejection of these claims, the Examiner states (Office Action, p. 3):

> In view of claim 9-10, 18-19 and 23, Feldmann et al. teaches a digital circuit from an integrated circuit, which determines the power coefficient of noise Pi, to predict a power spectral density P(s) from the digital circuit, but fails to discuss a mean bit rate. Chang et al. mentions mean bit rate as a method of determining new communication.
>
> Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the inventions to modify the power spectral density of Feldmann et al. with the deterministic method of Chang et al. with the expectation of determining a node for new communication. Chang et al. developed a method to determine whether or not a node was needed, which would utilize the mean bit rate data (Col. 4 lines 30-45).
>
> In view of claims 11,13, 20 and 22, Feldmann et al. discloses both a (*sic*) digital and analog circuits.

Applicants respectfully disagree. Independent claims 9 and 18 both describe methods for designing and fabricating integrated circuits. Accordingly, each of these claims comprises the steps of "fabricating said candidate integrated circuit when said power spectral density, *S(w)*, of said candidate digital circuit achieves a design goal for said candidate integrated circuit." Also see the Specification, p. 7 line 22 to p. 8, line 2. The fabrication of integrated circuits is not taught or suggested by the combination of Feldmann and Chang, nor does the Examiner argue that it is. In fact, neither Feldmann or Chang contain the words "fabrication" or "fabricate." Therefore, the subject matter as a whole of independent claims 9 and 18 would not have been obvious in light of this combination at the time the invention was made, and the claims should be allowed

In addition, the method of claim 18 further comprises "determining a mean bit rate, v, of said candidate digital circuit." In formulating the §103(a) rejection, the Examiner argues that this limitation is taught or suggested by Chang where "Chang et al. mentions mean bit rate as a method of determining new communication." Nevertheless, Chang only describes a "bit rate" associated with the rate of communication over a network. See, e.g., Chang, col. 3, lines 17-39. One skilled in the art would recognize that the "mean bit rate" described in the present invention, on the other hand, relates to the output of a digital circuit. See, e.g., the Specification, p. 4, line 15 - p. 5, line 20. Chang therefore does not teach or suggest this aspect of the present invention.

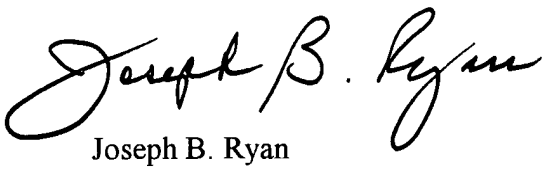
Moreover, the motivation for combining the Feldmann and Chang references in the §103(a) rejection is improper in light of the MPEP and recent case law from the Federal Circuit. The Federal Circuit has stated that when patentability turns on the questions of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual questions of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. Applicants respectfully submit that there has been no such showing in the present §103(a) rejections of such objective evidence of record that would motivate one skilled in the art to modify or combine the proposed references and reference combinations to design and fabricate integrated circuits. Instead the above quoted language is precisely the type of subjective, conclusory statements that the Federal Circuit has indicated provides insufficient support for an obviousness rejection.

Applicants submit that dependent claims 10, 11, 13, 19, 20, 22 and 23 are in condition for allowance for at least the same reasons stated above with respect to independent claims 9 and 18. Additionally, Applicants assert that these dependent claims contain separately patentable subject matter. For example, claims 11 and 20 describe methods of designing and fabricating and integrated circuits "wherein said candidate integrated circuit further comprises a candidate analog circuit." Neither Feldmann nor Chang teach or suggest the design and fabrication of an integrated circuit that comprises digital and analog circuits. In fact, neither reference even uses the word "analog." These claims, therefore, are not obvious in light of the Feldmann-Chang combination.

In view of the above, Applicants believe that claims 1-26 are in condition for allowance, and respectfully request the withdrawal of the §102(a) and §103(a) rejections.

A Notice of Appeal is submitted concurrently with these remarks.

Respectfully submitted,



Date: February 2, 2005

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Enclosure(s): Notice of Appeal